



1.4.3 Circuits

Q1

Draw a logic gate diagram to represent the Boolean expression.

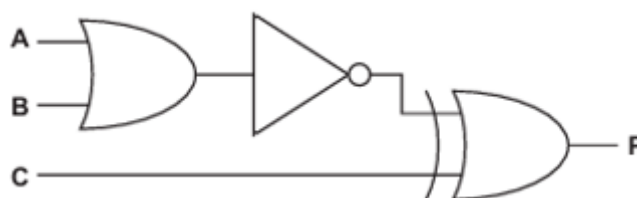
$$Q \equiv \neg A \vee B$$

[2 marks]



Q2

An engineer has created the following logic circuit.



- a) Give the Boolean expression that represents the logic circuit. Do not attempt to simplify the expression.

[2 marks]

- $\neg(A \vee B) \vee C$

- b) Complete the truth table for the logic circuit.

A	B	S	P
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

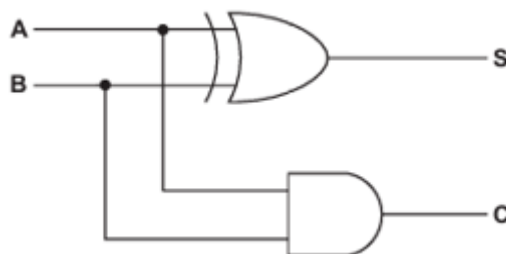
[2 marks]





Q3

The logic circuit below has two inputs (**A**, **B**) and two outputs (**S**, **C**).



a) Give the Boolean expressions for the outputs **S** and **C**.

[2 marks]

- $S \equiv A \vee B$
- $C \equiv A \wedge B$

b) Complete the truth table for the logic circuit.

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

[2 marks]

c) State the name of this circuit.

[1 mark]

- **Half Adder**

d) Describe how this logic circuit can be adapted to add together two 4-bit binary numbers.

[4 marks]

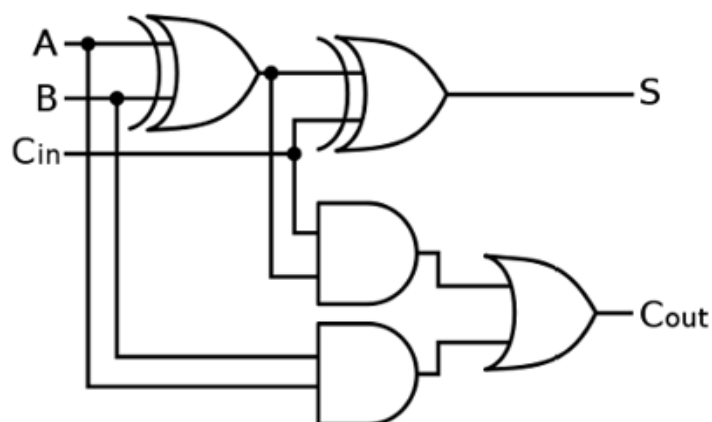
- **S gives the sum, C gives the carry**
- **Two half adders can be joined together...**
- **with an OR gate...**
- **to form a full adder**
- **4 full adders can be used to add two 4-bit binary numbers**
- **The carry out of adder is joined to the carry in of the next**





Q4

A diagram showing a full adder circuit is shown below.



a) Explain what the circuit does. You should refer to A, B, C_{in} , S and C_{out} in your answer.

[4 marks]

- The circuit adds two bits (and a carry bit) together
- A, B and C_{in} are added together
- The result is given by S
- And a carry bit by C_{out}

b) Complete the truth table below:

[4 marks]

A	B	C_{in}	S	C_{out}
1	1	1	1	1
1	1	0	0	1
1	0	1	0	1
1	0	0	1	0
0	1	1	0	1
0	1	0	1	0
0	0	1	1	0
0	0	0	0	0

c) Write a Boolean expression equivalent to S.

[1 mark]

- $S \equiv A \vee B \vee C_{in}$

d) Write a Boolean expression equivalent to C_{out} .

[2 marks]

- $C_{out} \equiv ((A \vee B) \wedge C_{in}) \vee (A \wedge B)$





e) Describe the difference between a half adder circuit and a full adder circuit.

[2 marks]

- A half adder can only add 2 single bits
- A full adder can handle a 3rd bit / a carry bit

Q5

A NAND gate and its truth table are shown below.



A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

a) Draw a set of gates equivalent to a NAND gate, but built only of AND, OR and NOT gates.

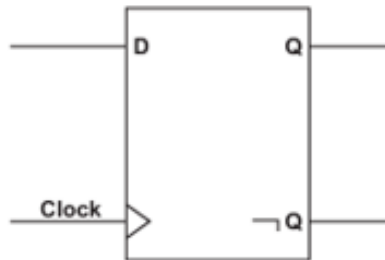
[2 marks]





Q6

The component below is a D-Type flip flop.

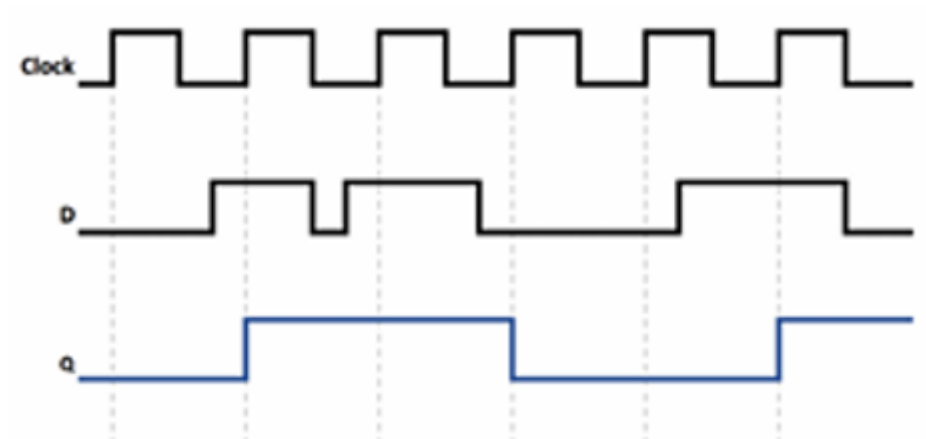


a) State the purpose of a flip-flop.

[1 mark]

- To store the state of a bit

b) Draw the output of the flip-flop below.



[3 marks]

