4.1.1 FDE Cycle

1 The processor contains registers including the accumulator and the program counter. The contents of these registers are modified during the Fetch-Decode-Execute cycle.

(a) Describe how the accumulator is used during the Fetch-Decode-Execute cycle.

[2 marks]

- **Holds the result of calculations from the ALU.**
- **Holds all inputs/outputs. (for LMC)**
- **Is checked during branching. (for LMC)**
- **Stores data which has come from the MDR/RAM. (for LMC)**

(b) Describe how the program counter is used during the Fetch-Decode-Execute cycle.

[2 marks]

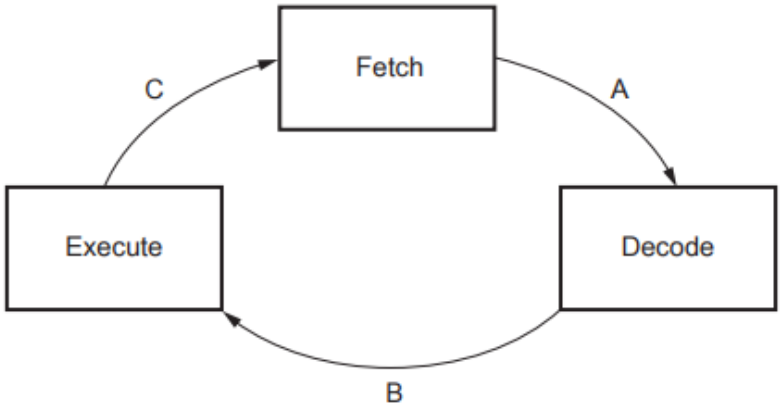
- **Holds the address of the next instruction.**
- **At the start of the fetch stage the contents is copied to the MAR.**
- **It is incremented after the instruction has been fetched**
- **Can be modified by branch instructions.**

(c) State the name of **three** other registers that are used during the Fetch-Decode-Execute cycle.

[3 marks]

- **Memory Address Register / MAR.**
- **Memory Data Register / MDR.**
- **Current instruction Register / CIR.**
- **Index Register / IR.**

2 A CPU will repeatedly run the Fetch-Decode-Execute-cycle shown below.



(a) Describe what happens during the 'Fetch' stage shown above.

You should refer to the use of specific registers in your answer.

[4 marks]

- **Data/address is copied from the PC to the MAR.**
- **Contents of MAR is passed onto the address bus.**
- **Memory read signal is sent onto the control bus.**
- **RAM copies the data from the location specified by the Address Bus onto the Data Bus.**
- **Data on the data bus is passed into the MDR.**
- **PC is incremented.**
- **Data is copied from the MDR to the CIR.**

(b) A CPU may need to stop running the Fetch-Decode-Execute-cycle in order to handle an interrupt.

Tick **one** box to indicate where an interrupt would be handled.

Fetch	
Decode	
Execute	✓

[1 mark]

3 State how each of the following components is used in the fetch phase of the fetch-decode-execute cycle:

(a) Program counter:

- **Stores the address of the next instruction.**
- **Is incremented between each instruction.**

(b) Memory address register

- **Stores the next memory location to be accessed.**

(c) Memory data register

- **Stores the data item fetched from/being sent to memory.**

(d) Current instruction register

- **Stores the current instruction that has been fetched.**
- **Holds the instruction while it is being decoded and executed.**

(e) Data bus

- **Transmits bidirectionally.**
- **Transmits data items/ instructions.**

(f) Address bus:

- **Transmits memory location to be accessed/read from/written to.**
- **Address bus accesses location stored in program counter/ memory address register.**

[6 marks]