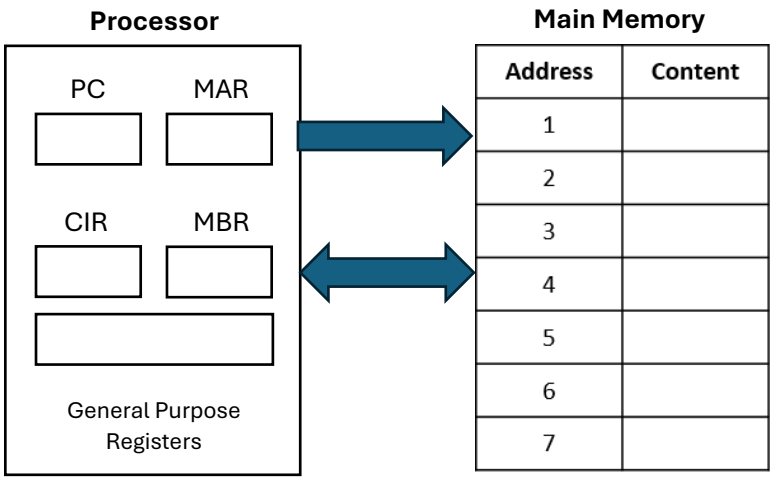
4.7.2 The Processor & the FDE Cycle

1) A **Figure 1** shows some of the internal components of a processor and how the processor is connected to main memory.

Figure 1



a) Describe how an instruction is fetched from main memory during the **fetch stage** of the fetch-decode-execute cycle.

[4 marks]

- **Contents of Program Counter(PC) is transferred to the Memory Address Register(MAR);**
- **The Address bus is used to transfer this address to main memory;**
- **The content of the addressed memory location is transferred using the data bus…;**
- **and loaded into the Memory Buffer Register(MBR);**
- **The contents of the MBR is copied to the Current Instruction Register(CIR);**

Ignore - Incrementing of PC

b) During the **decode and execute stages** of the FDE cycle the instruction that is being processed is stored in the CIR. Explain why the instruction could **not** be processed directly from the MBR.

[2 marks]

- **Executing the instruction may need additional data to be fetched from main memory**
- **Further memory fetches would overwrite the contents of the MBR**

Accept – MBR is not directly wired to all processor components needed to execute instructions

The computer system shown in **Figure 1** uses the von Neumann architecture. The Harvard architecture is an alternative to this.

c) Explain why the Harvard architecture is sometimes used in preference to the von Neumann architecture.

[2 marks]

- **Instructions and data can be accessed simultaneously**
- **Reduces the bottleneck of a single set of data/address buses**
- **Avoids possibility of data being executed as code**
- **Can use different types of memory for instructions and data.**
- **Instructions could use ROM to prevent the program being modified/hacked**
- **Instructions and data can have different word lengths**

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2) **Figure 2** shows the structure of an example machine code instruction, taken from the instruction set of a particular processor.

Figure 2

Opcode							**Operand**							
Basic Machine Operation						**Addressing Mode**								
0	1	1	0	1	1	0	1	0	0	1	1	0	1	1

a) State the purpose of the operand part of an instruction **and** explain how the addressing mode is related to this.

[2 marks]

- **An operand is a value/data that will be used by an operation**
- **The addressing mode indicates how the operand should be interpreted // whether the operand is a data value/memory location/register**

b) How many different basic machine operations could be supported by the instruction set of the processor in **Figure 2**.

[1 mark]

- 2^6 // 64

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3) **Figure 3** shows the format of a machine code instruction for a particular processor and one instruction in that format.

Figure 3

Opcode						Operand									
Basic Machine Operation					Addressing Mode										
1	0	1	1	0	1	0	1	1	0	1	0	0	0	0	1

a) If the operand can be used to refer to any location in the memory, how many memory locations can the processor address?

[1 mark]

- **2^{10} // 1024**

b) One of the two addressing modes that the processor supports is immediate addressing.

Explain what is meant by immediate addressing.

[1 mark]

- **The operand is the value that the instruction should apply the opcode to**

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4) Below is a definition of a term relating to the architecture of a computer system:

> Machine code instructions stored in main memory are fetched and executed serially by a processor that performs arithmetic and logical operations.

State which statement (A-D) below is the term that this definition defines.

A	The Harvard architecture
B	The processor instruction set
C	The stored program concept
D	The von Neumann architecture

[1 mark]

- **C**

5) Describe how the fetch-execute cycle is used to carry out machine code instructions.

Your response should include a description of what happens during each stage of the fetch-execute cycle.

[8 marks]

Fetch

- **Contents of the Program Counter/PC is transferred to the Memory Address Register/MAR**
- **Address bus is used to transfer this address to main memory**
- **Read signal is sent along the control bus**
- **Content of this memory address is transferred using the data bus**
- **And loaded into the Memory Buffer Register/MBR**
- **PC is incremented**
- **Contents of the MBR is copied to the Current Instruction Register/CIR**

Decode

- **Instruction to decode is held by the CIR**
- **The control unit decodes the instruction**
- **Instruction is split into opcode and operand**

Execute

- **Data may need to be fetched from or written to main memory**
- **The opcode identifies the type of operation/instruction to be performed**
- **The control unit sends control signals to coordinate the execution of the instruction**
- **Calculation/comparisons will use the Arithmetic Logic Unit(ALU) with the result in the accumulator(ACC)**
- **Status register may be updated**
- **Program counter is updated if a jump/branch is required**