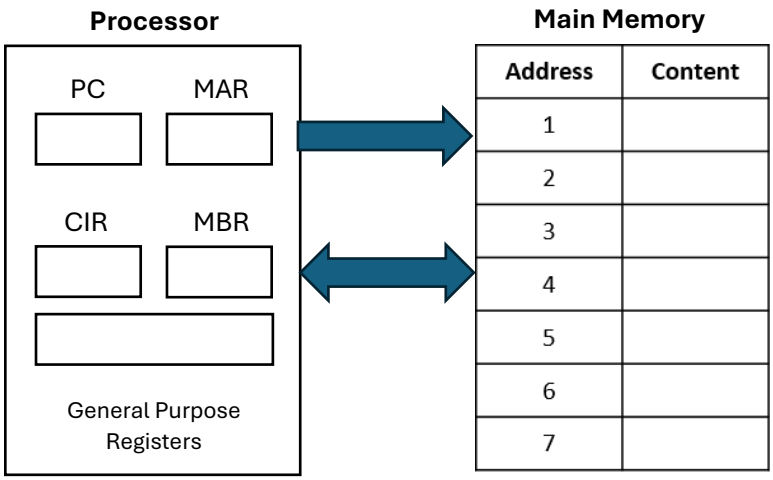
4.7.2 The Processor & the FDE Cycle

1) A **Figure 1** shows some of the internal components of a processor and how the processor is connected to main memory.

Figure 1



a) Describe how an instruction is fetched from main memory during the **fetch stage** of the fetch-decode-execute cycle.

[4 marks]

b) During the **decode and execute stages** of the FDE cycle the instruction that is being processed is stored in the CIR. Explain why the instruction could **not** be processed directly from the MBR.

[2 marks]

The computer system shown in **Figure 1** uses the von Neumann architecture. The Harvard architecture is an alternative to this.

c) Explain why the Harvard architecture is sometimes used in preference to the von Neumann architecture.

[2 marks]

2) **Figure 2** shows the structure of an example machine code instruction, taken from the instruction set of a particular processor.

Figure 2

Opcode							Operand							
Basic Machine Operation						Addressing Mode								
0	1	1	0	1	1	0	1	0	0	1	1	0	1	1

a) State the purpose of the operand part of an instruction **and** explain how the addressing mode is related to this.

[2 marks]

b) How many different basic machine operations could be supported by the instruction set of the processor in **Figure 2**.

[1 mark]

---

3) **Figure 3** shows the format of a machine code instruction for a particular processor and one instruction in that format.

Figure 3

Opcode						Operand									
Basic Machine Operation					Addressing Mode										
1	0	1	1	0	1	0	1	1	0	1	0	0	0	0	1

a) If the operand can be used to refer to any location in the memory, how many memory locations can the processor address?

[1 mark]

b) One of the two addressing modes that the processor supports is immediate addressing.

Explain what is meant by immediate addressing.

[1 mark]

---

4) Below is a definition of a term relating to the architecture of a computer system:

> Machine code instructions stored in main memory are fetched and executed serially by a processor that performs arithmetic and logical operations.

State which statement (A-D) below is the term that this definition defines.

A	The Harvard architecture
B	The processor instruction set
C	The stored program concept
D	The von Neumann architecture

[1 mark]

---

5) Describe how the fetch-execute cycle is used to carry out machine code instructions.

Your response should include a description of what happens during each stage of the fetch-execute cycle.

[8 marks]
