4.6.4 Logic Gates

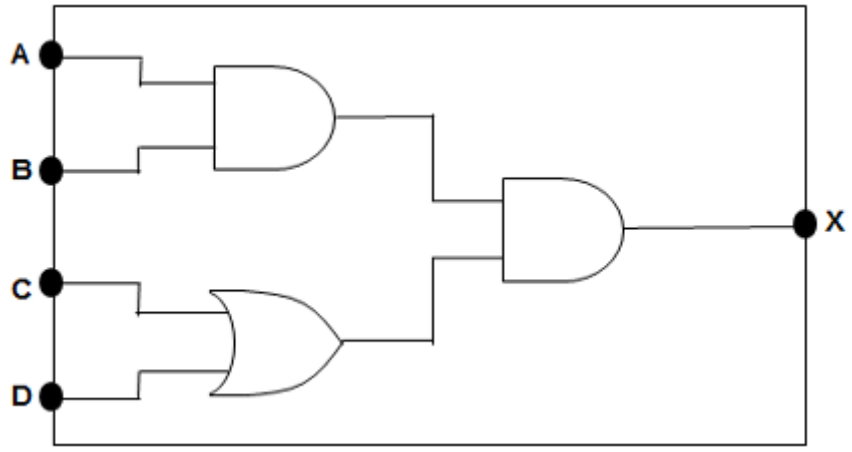
1) A computer process, X, can only start executing once processes A and B have finished executing and either communication channel C or communication channel D or both are available to use.

The states of processes and communication channels can be read using the following Boolean variables:

- **A** is set to TRUE if process A has completed and FALSE if it is still running.
- **B** is set to TRUE if process B has completed and FALSE if it is still running.
- **C** is set to TRUE if communication channel C is available and FALSE if it is not available.
- **D** is set to TRUE if communication channel D is available and FALSE if it is not available.

a) Draw a logic circuit that will represent the logic of the system described above for the inputs **A**, **B**, **C** and **D** and the output **X**

[3 marks]



b) Write a Boolean expression to represent the logic used to start process X.

[2 marks]

- $X = A \cdot B \cdot (C + D)$

2) D-type flip-flops can be included in logic circuits.

a) Explain the general purpose of a D-type flip-flop.

[1 mark]

- **Used to store state of data input // used as a memory unit**

b) One input to a D-type flip-flop is a data signal. State what the other input to a D-type flip-flop is **and** what it is used for.

[2 marks]

- **The input is a clock signal**
- **It is used to store the state of the data input**

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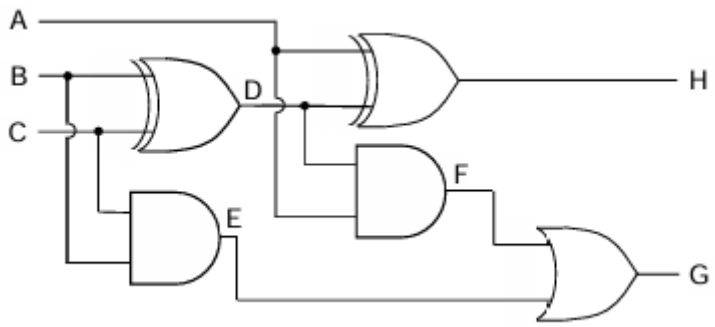
3) **Figure 1** shows a logic circuit.

Figure 1



a) Complete the truth table below for the circuit in **Figure 1**.

Inputs						Outputs	
A	**B**	**C**	**D**	**E**	**F**	**G**	**H**
0	0	0	**0**	**0**	**0**	**0**	**0**
0	0	1	**1**	**0**	**0**	**0**	**1**
0	1	1	**0**	**1**	**0**	**1**	**0**
1	1	1	**0**	**1**	**0**	**1**	**1**

[3 marks]

b) Using figure 5, write a Boolean expression to show how the output **G** is calculated form the inputs **A**, **B** and **C**.

[3 marks]

- $B \cdot C + A \cdot (B \oplus C)$

c) Explain the purpose of the circuit.

[1 mark]

- **It adds together its inputs // it is a full adder circuit**

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4) Complete the truth tables for the OR and NAND gates.

OR Gate

Inputs		Output
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**1**

NAND Gate

Inputs		Output
0	0	**1**
0	1	**1**
1	0	**1**
1	1	**0**

[1 mark]

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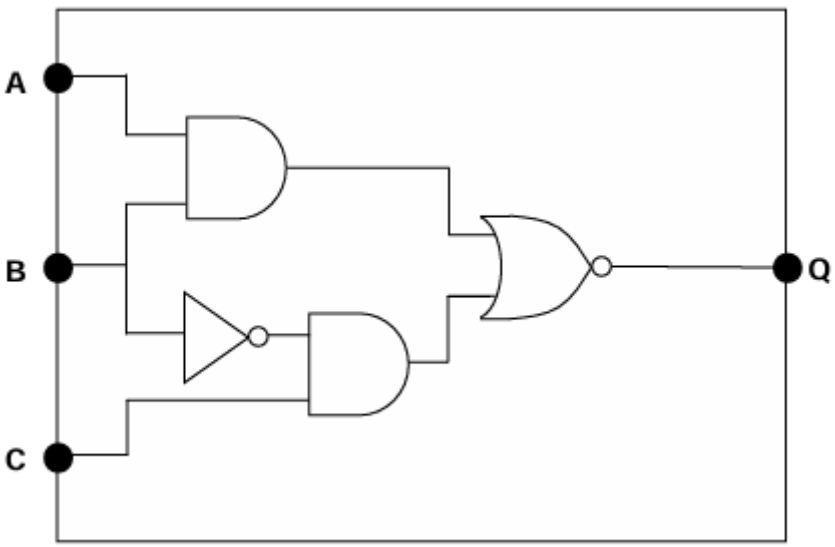
5) Draw the logic circuit for the Boolean expression:

$$Q = \overline{(A \cdot B + C.\overline{B})}$$



[4 marks]

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6) Which table below (**A**-**D**) **does not** represent one of the logic gates: OR, XOR, NOR.

Table A

Inputs		Output
0	0	1
0	1	0
1	0	0
1	1	0

Table B

Inputs		Output
0	0	0
0	1	1
1	0	1
1	1	0

Table C

Inputs		Output
0	0	1
0	1	0
1	0	0
1	1	1

Table D

Inputs		Output
0	0	0
0	1	1
1	0	1
1	1	1

[1 mark]

- **C**

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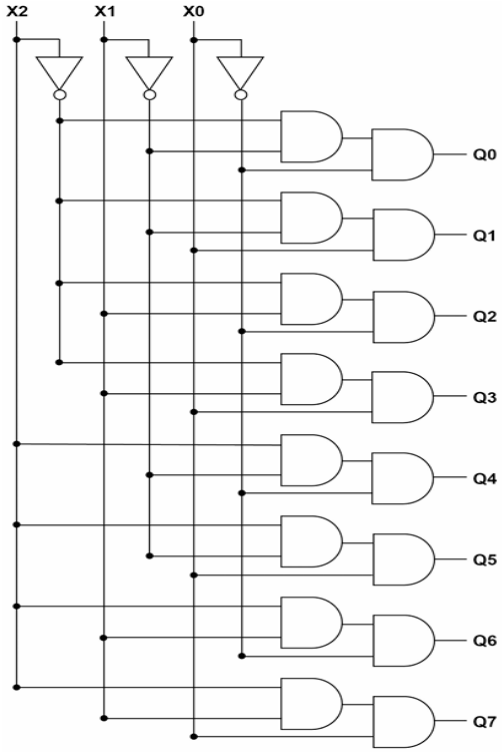
7) **Figure 2** shows a circuit with inputs **X0** to **X2** and outputs **Q0** to **Q7**.

Figure 2



a) Write a Boolean expression to represent the output **Q1** of the circuit in **Figure 2**.

[1 mark]

- $Q1 = \overline{X2} \cdot \overline{X1} \cdot X0$

b) Complete the truth table below for the circuit in **Figure 2**.

Inputs			Outputs							
X2	**X1**	**X0**	**Q0**	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**
0	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0	0	1	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**
0	1	0	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**
0	1	1	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
1	0	0	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**
1	0	1	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**
1	1	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
1	1	1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

[3 marks]

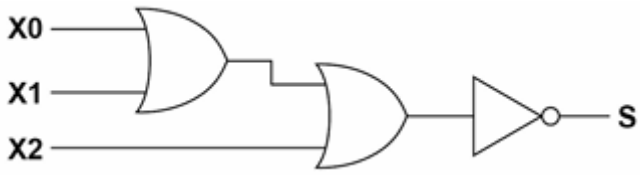
c) Explain the purpose of the circuit in **Figure 2**.

[2 marks]

- **Output Qn is 1 when the binary pattern input is the value n**
- **It converts a binary input to a decimal output**

d) The logic circuit in **Figure 3** produces an output **S** that is equivalent to one of the outputs of the logic circuit in **Figure 2**, for the inputs **X0**, **X1** and **X2**.

Figure 3



Which output (**Q0** to **Q7**) from **Figure 2** is the output **S** from the circuit in **Figure 3** equivalent to?

[1 mark]

- **Q0**

8) The truth table in **Table 1** represents the operation of a logic system.

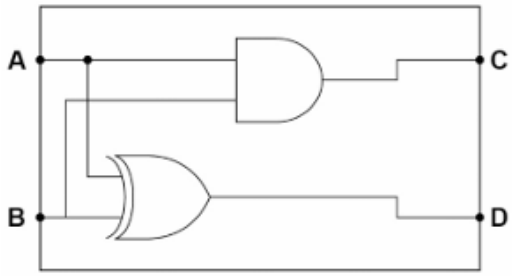
Table 1

Inputs		Outputs	
A	**B**	**C**	**D**
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

a) Draw a logic circuit that would produce the outputs shown in **Table 1** for the given inputs.

To achieve full marks for your response, your circuit should use **exactly two gates**.

[3 marks]



b) Explain the purpose of the circuit that you have drawn that produces the outputs given in **Table 1**.

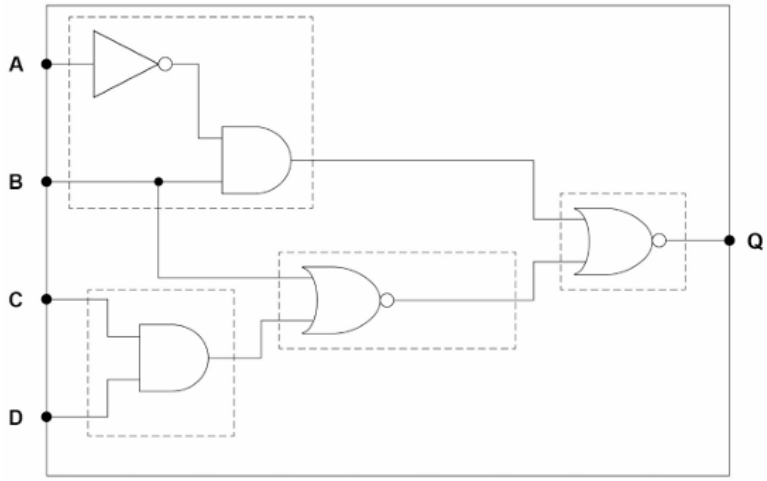
[1 mark]

- **It adds two bits together // it is a half adder**

9) Draw the logic circuit for the Boolean expression:

$$Q = \overline{\overline{A} \cdot B + \overline{B + C \cdot D}}$$

Do **not** simplify the expression.



[4 marks]

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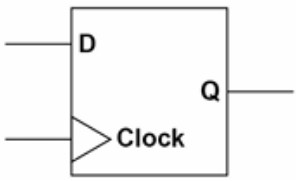
10) A flip-flop is a component that can be incorporated into a logic circuit. **Figure 4** shows a diagram of an edge-triggered D-type flip-flop.

Figure 4



Explain how the output **Q** will be affected when a pulse is received on the **Clock** input.

[1 mark]

- **Output Q will change to reflect current value of D**

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11) A burglar alarm system is to be implemented that has the following sensors:

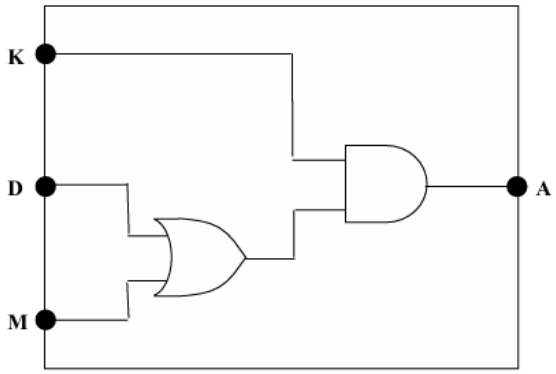
- A door sensor **D** that outputs TRUE when the door is open and FALSE when the door is shut
- A pressure mat sensor **M** that outputs TRUE while a weight is detected on it and FALSE when no weight is detected on it.

The alarm also has a key **K** that turns the alarm on and off. **K** outputs a TRUE signal when the alarm is switched on and FALSE when the alarm is off.

The alarm output **A** sounds a bell. It should be TRUE if:

- The alarm is on AND
- Either of the sensors **D** or **M** are set to the value TRUE.

a) In the space below, draw a logic circuit that will behave as described above for the inputs **D**,**M** and **K** and the output **A**.



[2 marks]

b) Write a Boolean expression to represent the logic of this alarm system.

[2 marks]

- $A = (D + M) \cdot K$

c) In this alarm system, the alarm bell will sound only while the door is open or a weight is placed on the pressure mat. If someone who has stepped on to the mat moves off it, or an open door is closed, the alarm bell will stop ringing.

A D-type flip-flop could be incorporated into the logic circuit so that the alarm bell would continue to sound after a person closed the door or moved off the pressure mat.

Explain how this could be achieved. In your answer refer to:

- why a D-type flip-flop would be suitable for this task
- where the D-type flip-flop would need to be inserted into the circuit
- what additional input the D-type flip-flop would need.

[3 marks]

- **Flip-flop will store the state of its input // Flip-flop acts as memory**
- **Insert into circuit between the output of the OR gate and the AND gate // after the AND gate**
- **Clock signal // trigger // signal to indicate when the value (of the input) should be stored/read**

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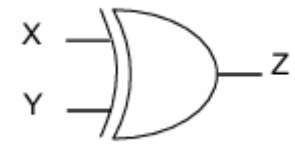
12) What is the name of the logic gate represented by the truth table and symbol shown in **Figure 5**?

Figure 5

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	0



[1 mark]

- **XOR**

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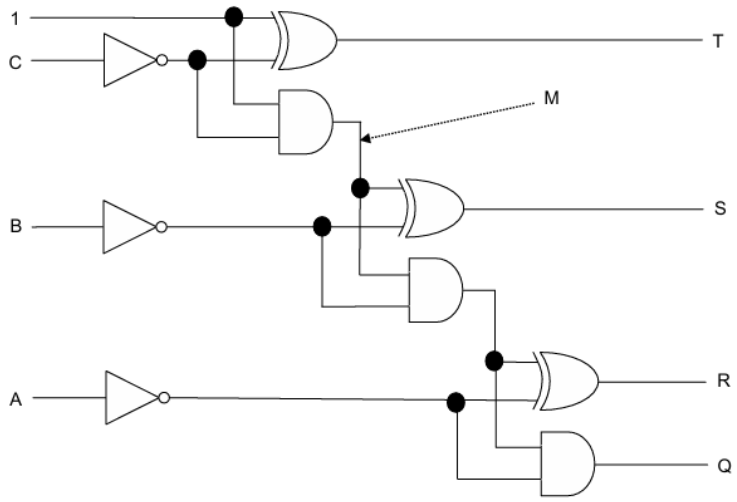
13) **Figure 6** shows a logic circuit that might be found inside a processor?

Figure 6



a) The value at M (indicated by the arrow in Figure 6) is represented by the following Boolean expression.

$$1 \cdot \overline{C}$$

Simplify this Boolean expression.

[1 mark]

- $\overline{C}$

b) The output T is represented by the following Boolean expression.

$$1 \oplus \overline{C}$$

Simplify this Boolean expression.

[1 mark]

- C

c) Complete the missing cells in **Table 2**.

Table 2

Inputs			Outputs		
C	**B**	**A**	**T**	**S**	**R**
0	0	0	0	0	0
0	0	1	**0**	**0**	**1**
0	1	0	**0**	**1**	**1**
0	1	1	0	1	0

[3 marks]

d) The logic circuit shown in **Figure 6** obtains the two's complement of a 3-bit binary number. Explain how this circuit could be used by a processor when subtracting one 3-bit binary number from another.

[1 mark]

- **Use this circuit on the binary number to be subtracted and add the result to the other binary number**